**Digital Design and Computer Organization Laboratory**

**UE21CS251A**

**3rd Semester, Academic Year 2022-23**

Date:2/09/2022

|  |  |  |
| --- | --- | --- |
| Name: Abhishek V Sagarnal | SRN:PES2UG21CS023 | Section  A |

Week#\_\_3\_\_\_\_\_\_\_\_\_

Program Number :\_\_\_1\_\_\_\_

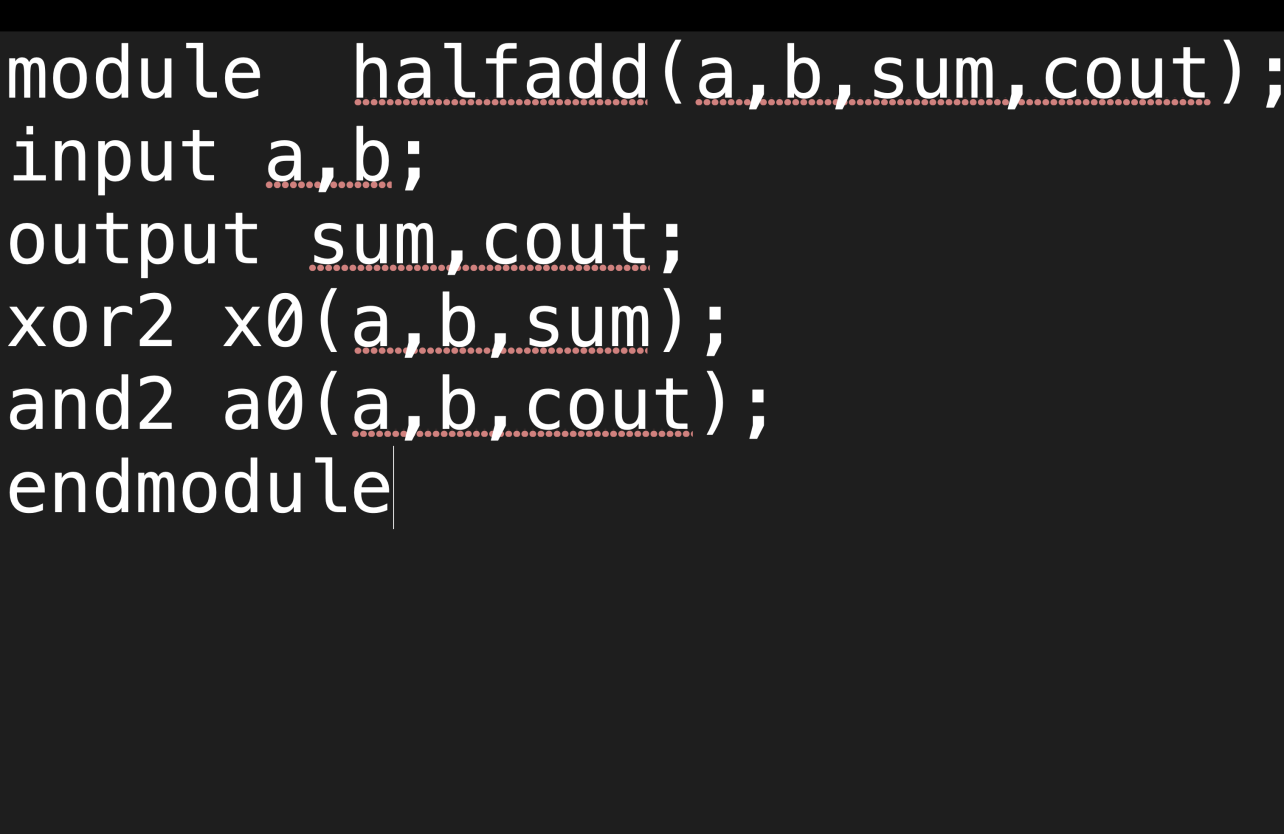
Title of the Program

**Half Adder**

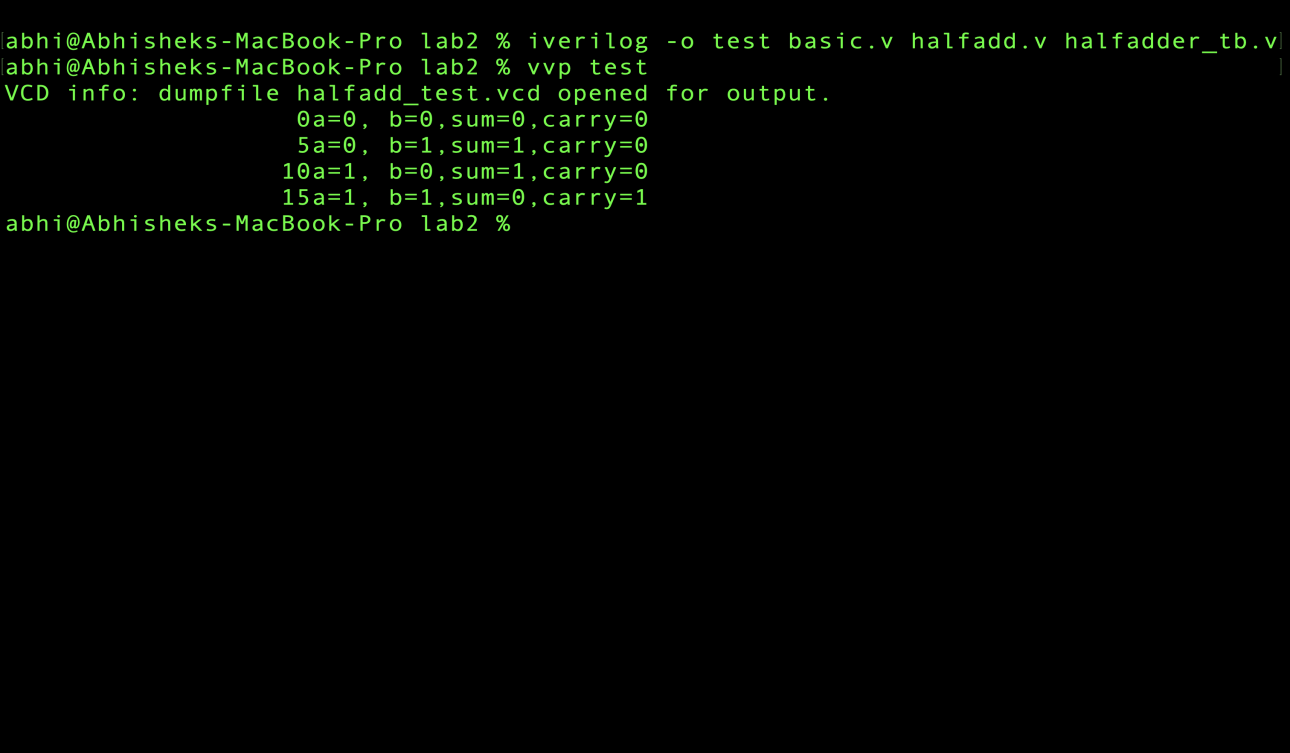
Aim:

**WRITE A VERILOG PROGRAM TO MODEL THE HALF ADDER. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE**

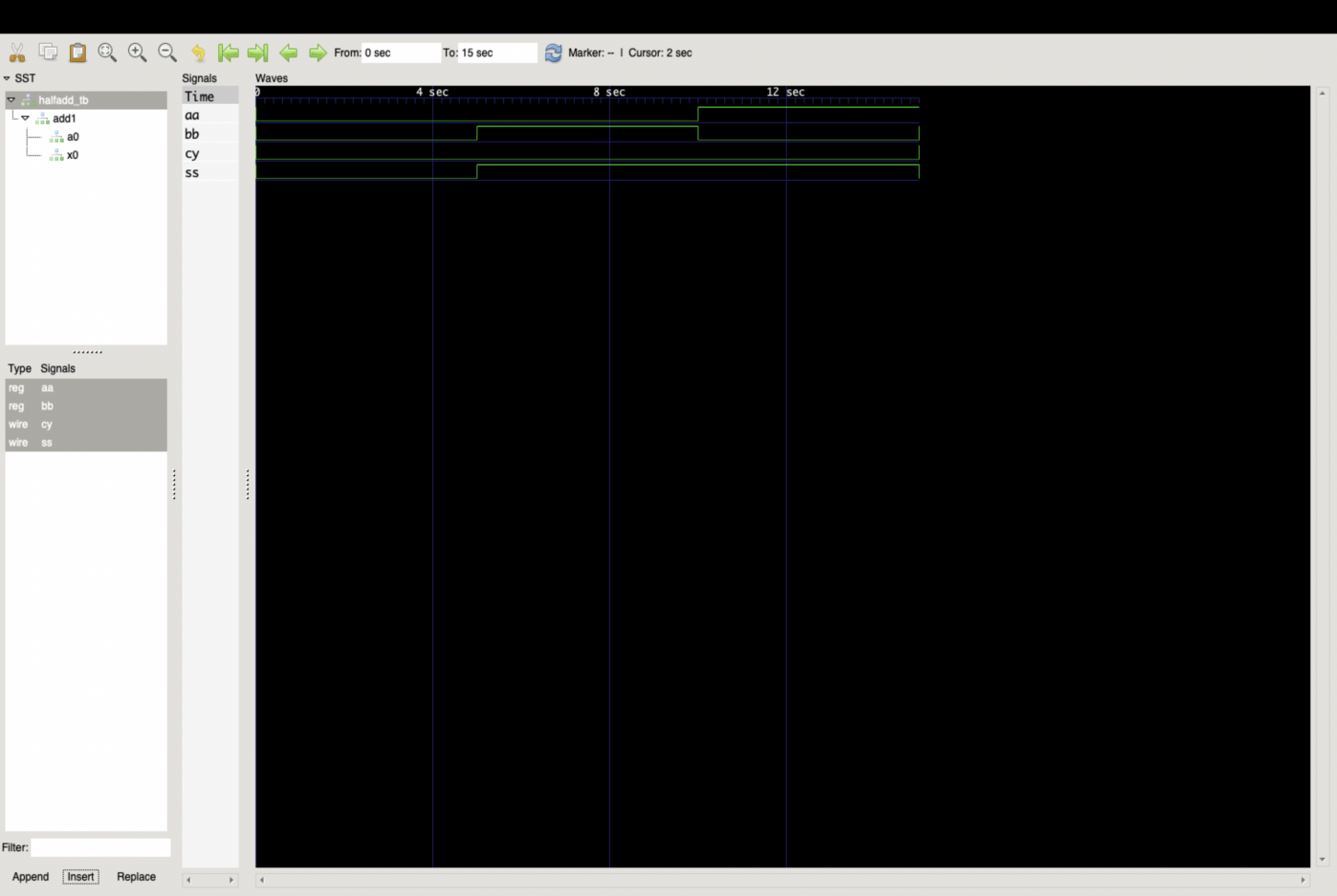
1. Paste the Screen Shot of the source code



1. Paste the Screen Shot of the VVP command output



1. Paste the Screen shot of the GTKWave form



1. Include relevant Truth Table

|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **sum** | **carry** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |

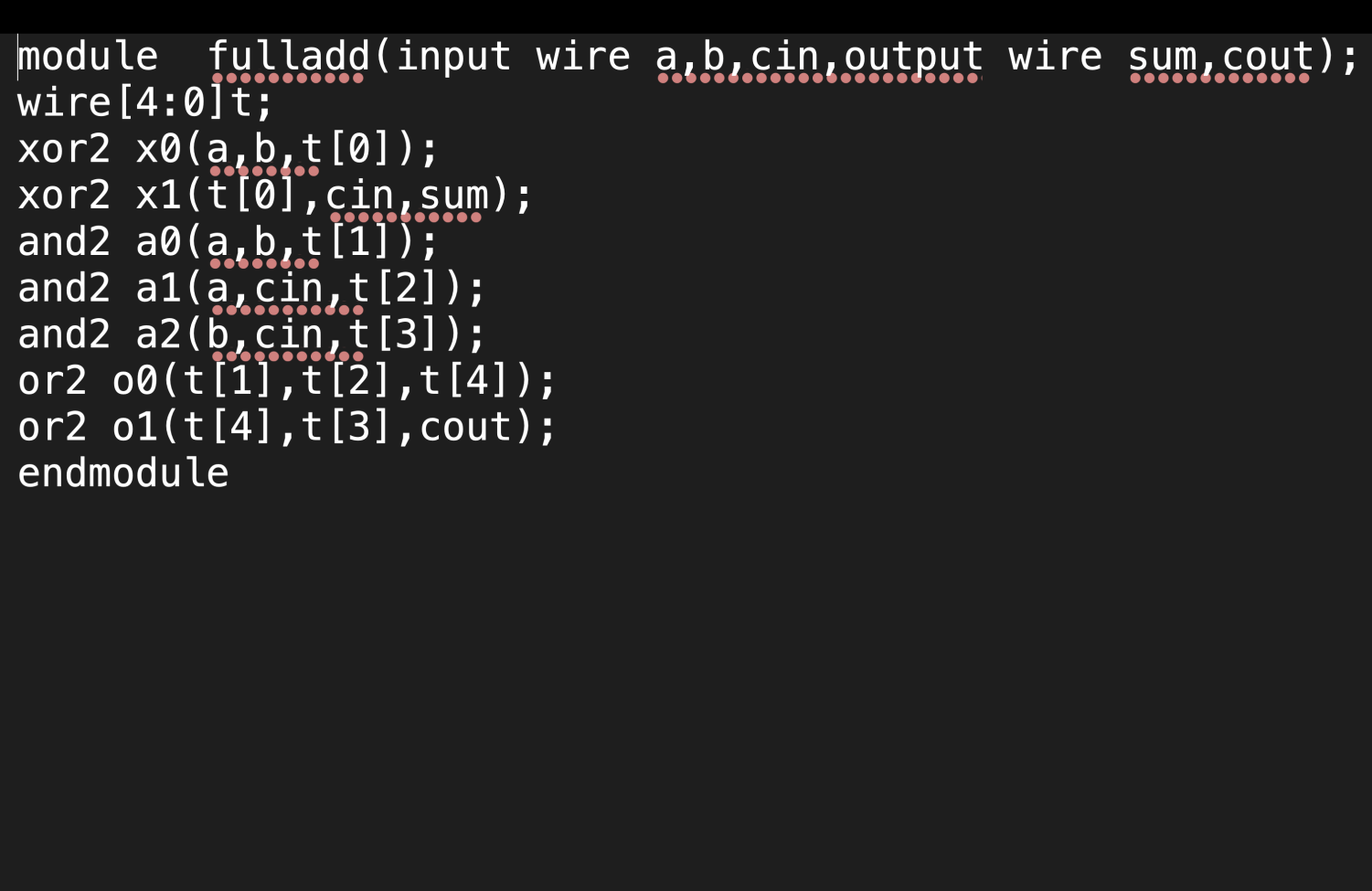
Program Number :\_\_\_2\_\_\_\_

Title of the Program

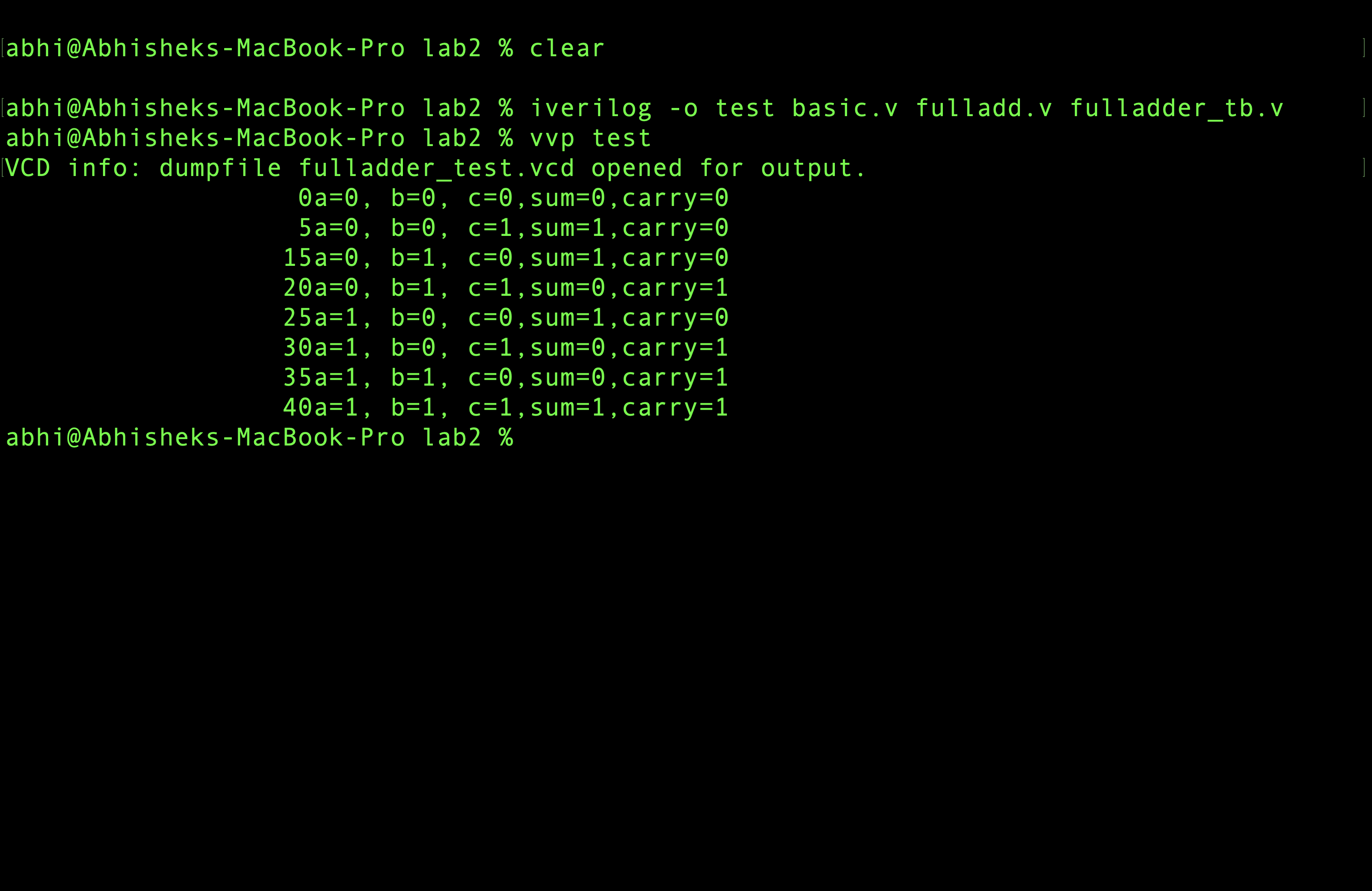
**FULL ADDER**

**WRITE A VERILOG PROGRAM TO MODEL THE FULL ADDER. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE**

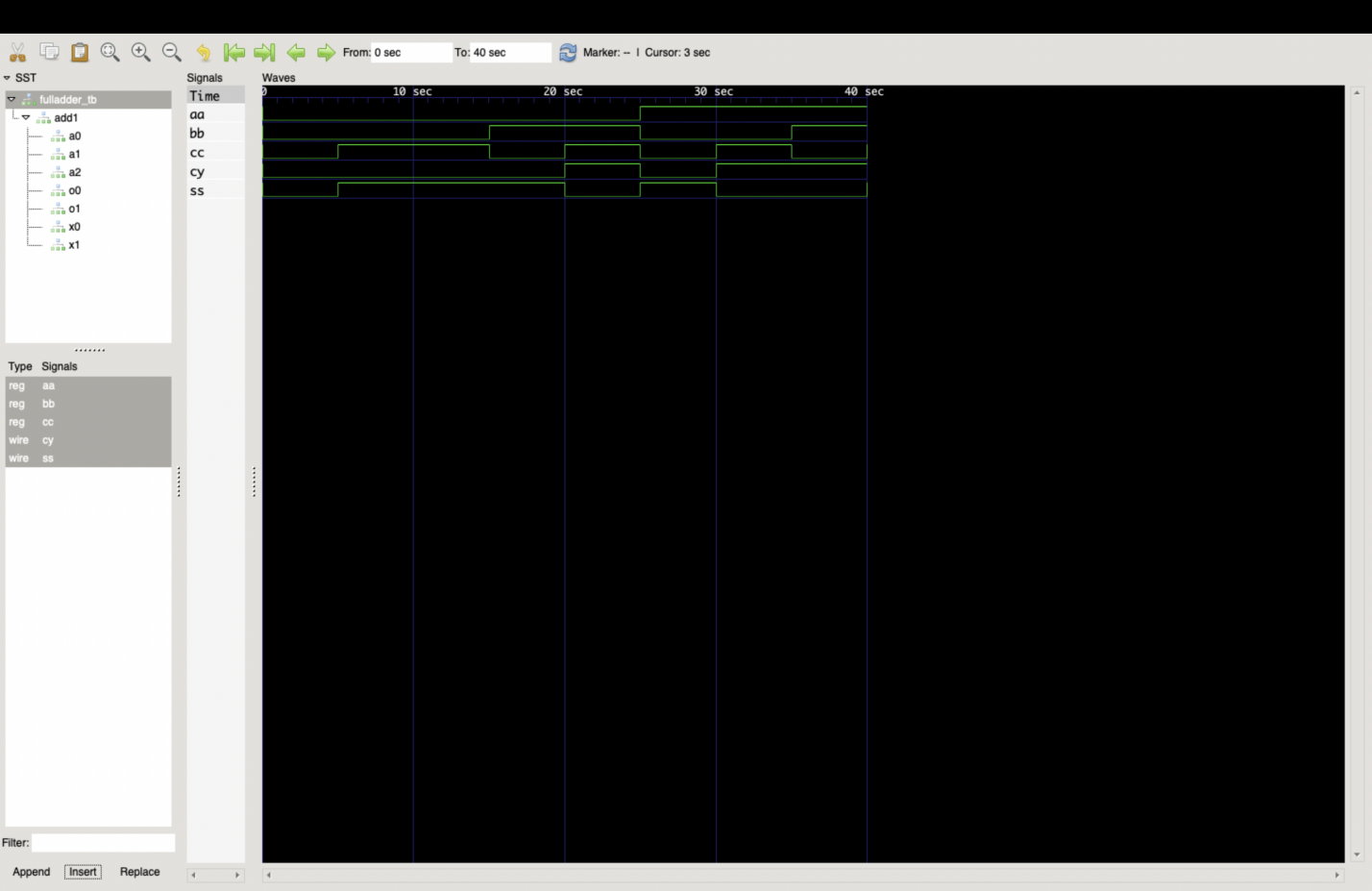
1. Paste the Screen Shot of the source code



1. Paste the Screen Shot of the VVP command output



1. Paste the Screen shot of the GTKWave form



1. Include relevant Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **a** | **b** | **c** | **sum** | **carry** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **1** | **1** |

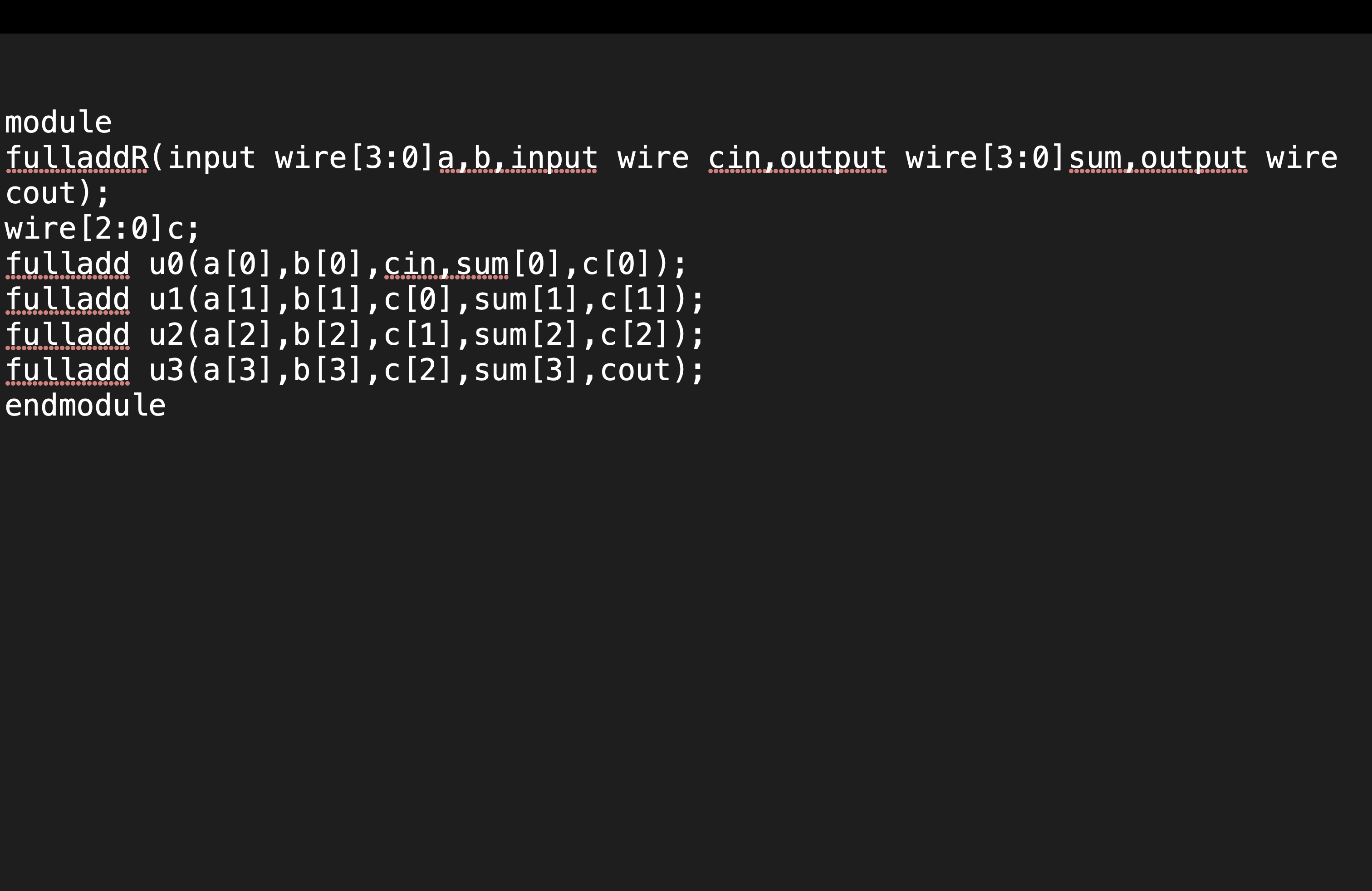
Program Number :\_\_\_3\_\_\_\_

Title of the Program

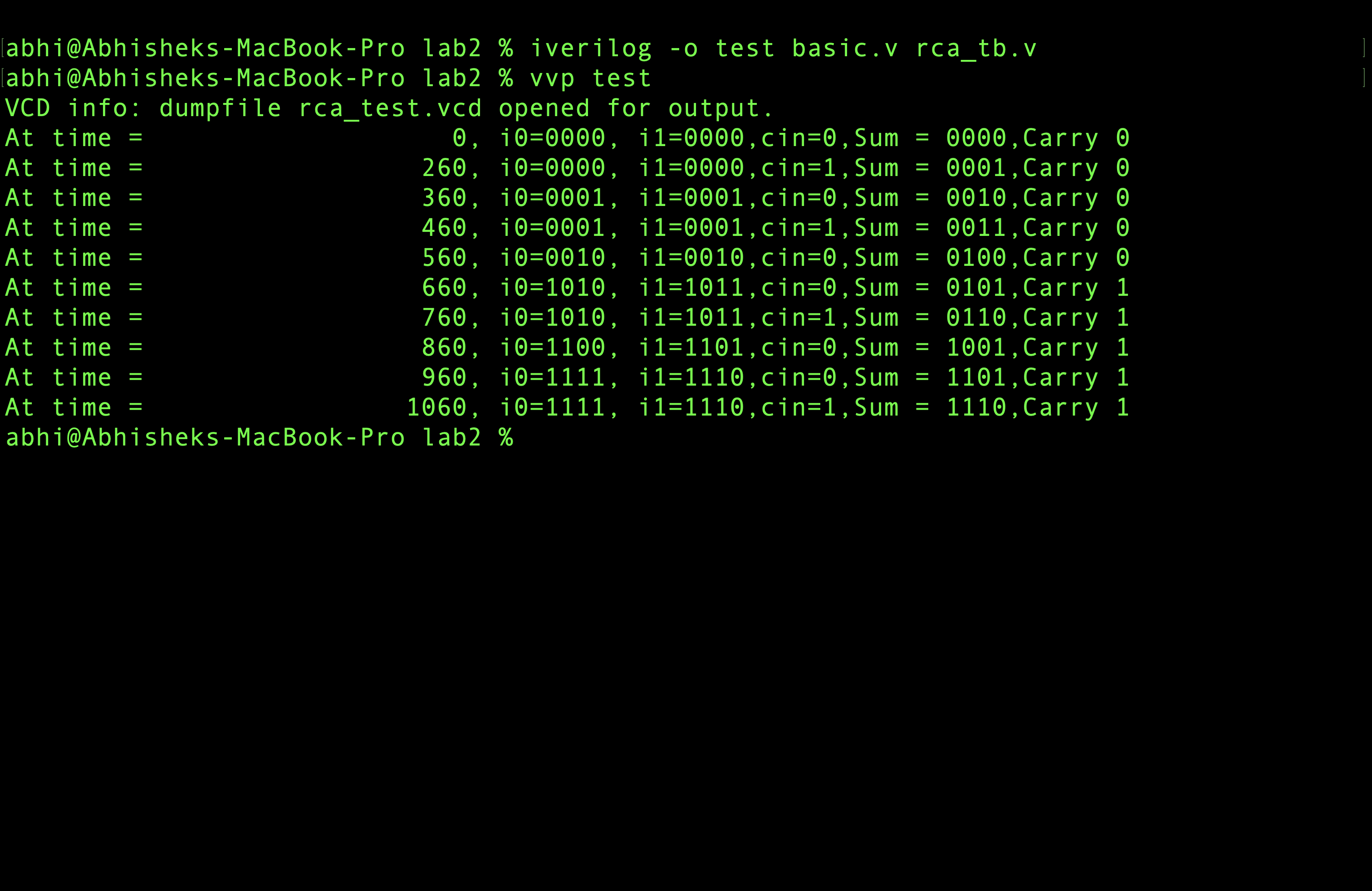
**4 BIT RIPPLE CARRY ADDER**

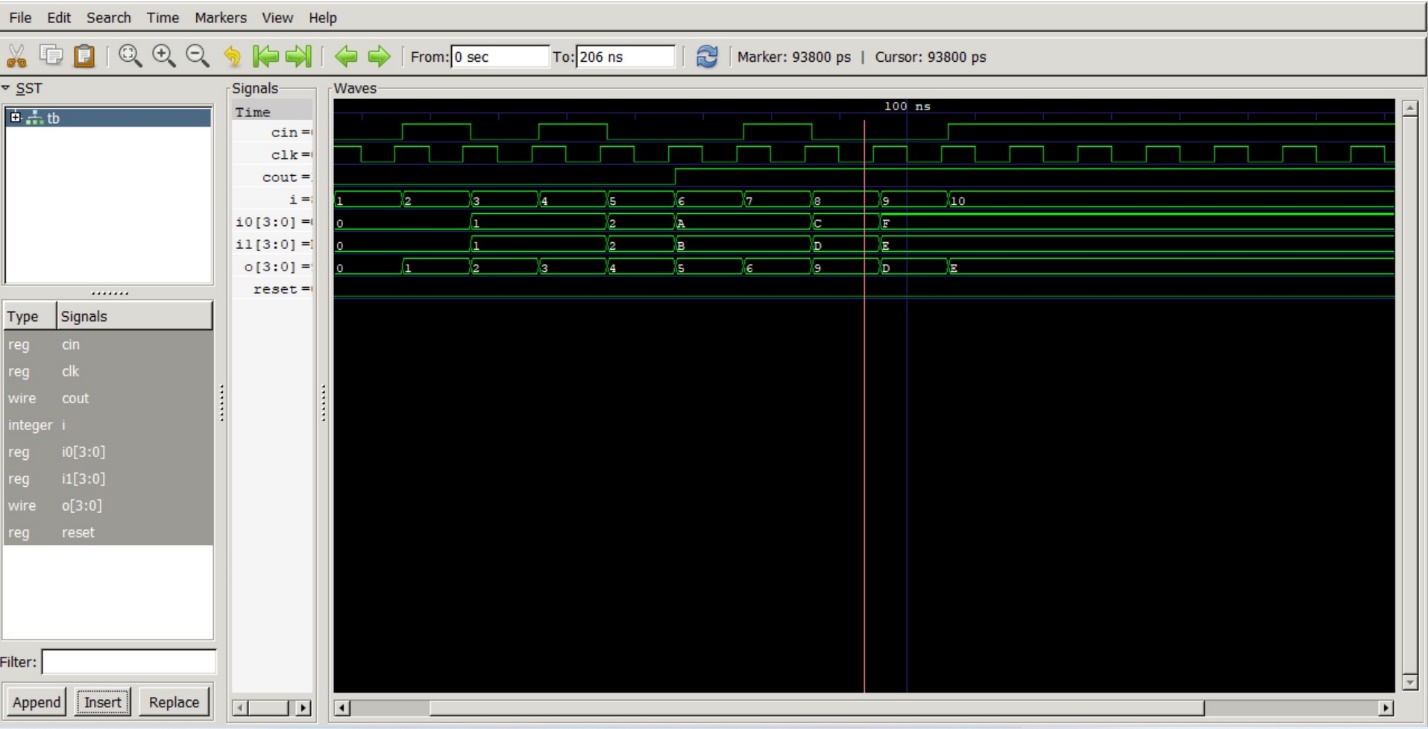
**WRITE A VERILOG PROGRAM TO MODEL THE 4 BIT RIPPLE CARRY ADDER. GENERATE THE VVP OUTPUT AND VIEW THE SIMULATION WAVEFORM USING GTKWAVE.VERIFY THE OUTPUT AND WAVEFORM WITH THE RELEVANT TRUTH TABLE**

1. Paste the Screen Shot of the source code



1. Paste the Screen Shot of the VVP command output



1. Paste the Screen shot of the GTKWave form****
2. Include relevant Truth Table:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **time** | **Io** | **I1** | **cin** | **sum** | **carry** |
| **0** | **0000** | **0000** | **0** | **0000** | **0** |
| **260** | **0000** | **0000** | **1** | **0001** | **0** |
| **360** | **0001** | **0001** | **0** | **0010** | **0** |
| **460** | **0001** | **0001** | **1** | **0011** | **0** |
| **560** | **0010** | **0010** | **0** | **0100** | **0** |
| **660** | **1010** | **1011** | **0** | **0101** | **1** |
| **760** | **1010** | **1011** | **1** | **0110** | **1** |
| **860** | **1100** | **1101** | **0** | **1001** | **1** |
| **960** | **1111** | **1110** | **0** | **1101** | **1** |
| **1060** | **1111** | **1110** | **1** | **1110** | **1** |

**Disclaimer:**

* The programs and output submitted is duly written, verified and executed my me.
* I have not copied from any of my peers nor from the external resource such as internet.
* If found plagiarized, I will abide with the disciplinary action of the University.

Signature:A..V.S

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Section: A

Date:2/09/2022